O.P.Code: 18CS0505 | R18 | H.T.No.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester Supplementary Examinations June-2024
COMPUTER ORGANIZATION & ARCHITECTURE
(Common to CSE & CSIT)

Time: 3 Hours **Max. Marks: 60**

PART-A
(Answer all the Questions **5 x 2 = 10** Marks)

1	a	What are the types of Addressing modes?	CO1	L1	2M
	b	What are the different types of data representation?	CO2	L1	2M
	c	Compare hardwired control unit with micro programmed control unit.	CO3	L2	2M
	d	Draw the diagram IO subsystem.	CO4	L2	2M
	e	Define pipelining and mention various interconnection structures.	CO5	L1	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Write in detail about Data Manipulation Instructions with examples.	CO1	L1	5M
	b	List the types of instruction sets available with suitable example instructions.	CO1	L2	5M

OR

3	a	Write about input-output subsystems with neat diagrams?	CO1	L1	5M
	b	With a neat sketch discuss about the Functional Units of Computer.	CO1	L2	5M

UNIT-II

4		Outline the H/W Flowchart and write algorithm for Division non-restoring with an Example.	CO2	L2	10M

OR

5		Interpret the step by step signed-operand multiplication process using Booth's algorithm When (-9) and (-13) are multiplied.Assume 5-bit registers to hold signed numbers and (-9) to be the multiplicand.	CO2	L3	10M

UNIT-III

6	a	Explain the concept of Register Transfer Logic (RTL) with suitable diagram.	CO3	L1	5M
	b	Explain the way of constructing a 4-line common bus system with a neat diagram.	CO3	L1	5M

OR

7	a	"Micro pragrammed unit is slower than hardwired unit" justify the statement.	CO3	L2	5M
	b	Write in detail about Logic Micro Operations with neat representations?	CO3	L2	5M

UNIT-IV

8		Consider the following Page reference string: 7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1,7,0,1. Explain the FIFO and LRU page replacement algorithms.	CO4	L3	10M

OR

9	a	Discuss about any two memory mapping procedures in cache memory.	CO4	L2	6M
	b	Explain the working of DMA.	CO4	L2	4M

UNIT-V

10	a	Draw 8×8 omega switching network with explanation.	CO5	L1	4M
	b	Define parallel processing? How one can achieve parallel processing with single CPU?	CO5	L2	6M
		OR			
11	a	Discuss about throughput and speed up of pipelining?	CO5	L2	5M
	b	Describe the cache coherency in detail.	CO5	L2	5M

***** END *****